

Design rules

PCB – rigid, flex & rigid-flex

Eurotronics produces highly **advanced printed circuit board technologies** to the unique requirements of each customer.

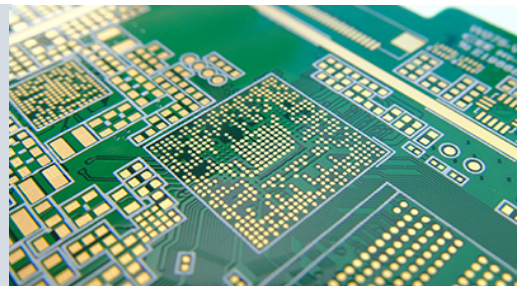
Beside standard printed circuit board technologies, Eurotronics adapts to the ongoing market trend toward miniaturization demands: ever thinner and ever more highly integrated printed circuit boards. We offer advanced capabilities ranging from ultra-fine line production with copper filled stacked micro vias to the processing of ultra-thin base materials and the manufacture of complex rigid-flex substrates incorporating bookbinder and window technology.

Our partner production facility is perfectly equipped to build highly integrated (HDI) multi-layer rigids and complex flexible circuit boards, suitable for COB, COF, flip chip and wire bond applications.

In order to achieve optimal quality results, we advise to follow the applicable design rules and the designated IPC standards. This technical information only represents our basic capabilities. Together with our engineers we will evaluate our customer's layout designs to work out the best possible solution.

Standard

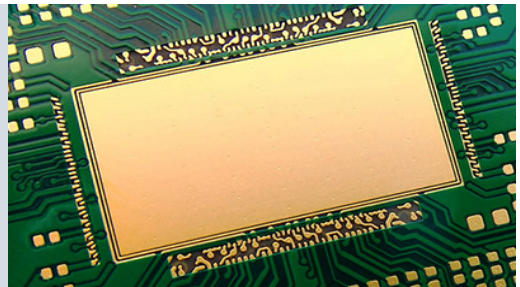
To enable achieving highest level of production yields and product reliability, the design values mentioned in the standard category should be followed whenever possible for layout designs.



Advanced

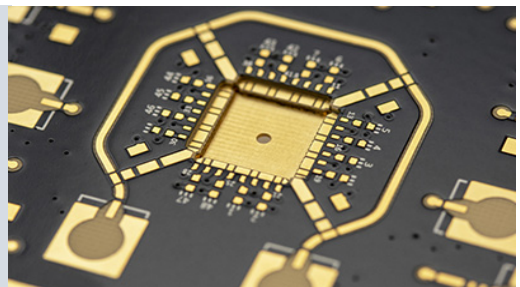
To achieve design values in this category, special materials, processes and equipments might be needed.

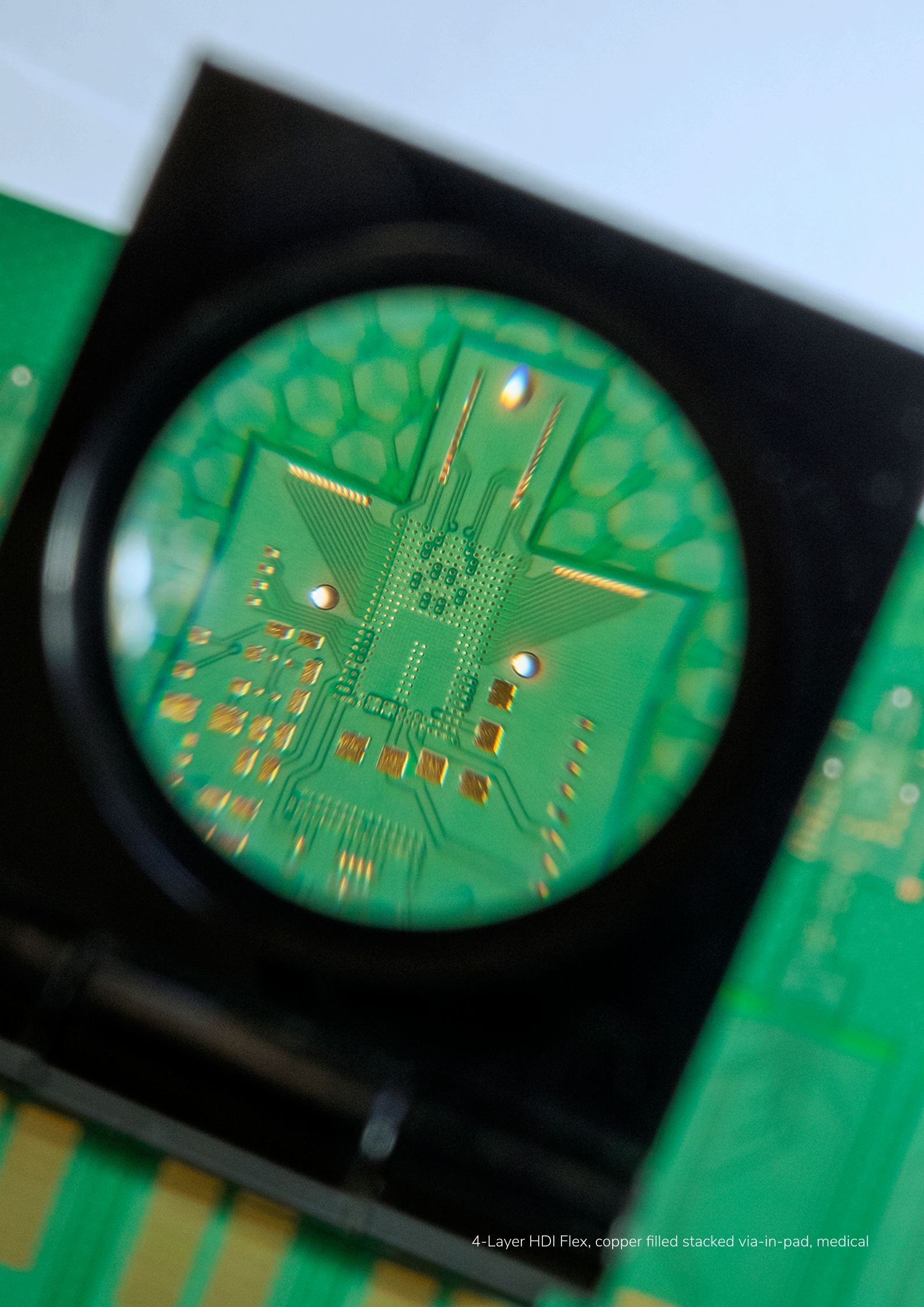
If the design values of this category are intended to be used, Eurotronics strongly recommends consulting its engineering teams during the early design phase (Design for Manufacturing).



Development

Eurotronics' engineering teams are looking forward to support your development projects. Design values that go beyond the ones mentioned in the categories "standard" and "advanced" are considered to have development status. PCBs designed using values of this category will require high level attention of our engineering teams.

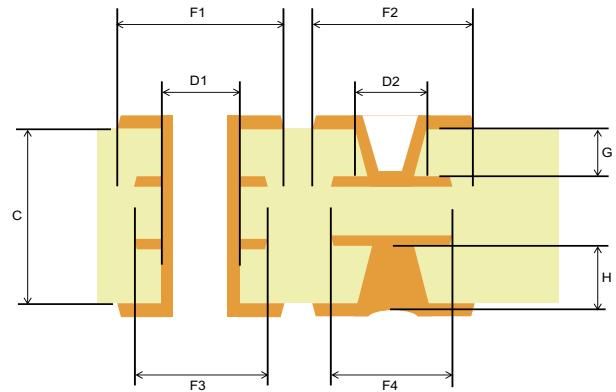
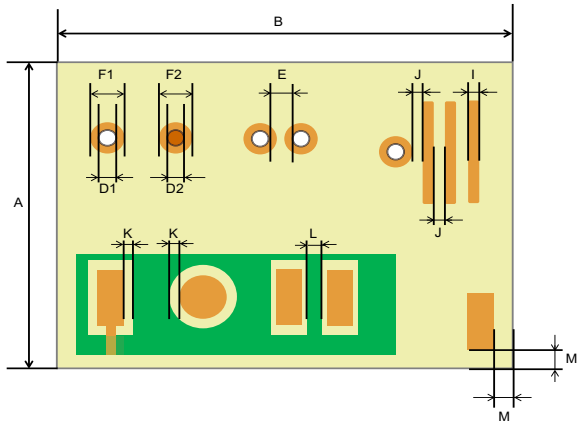




4-Layer HDI Flex, copper filled stacked via-in-pad, medical

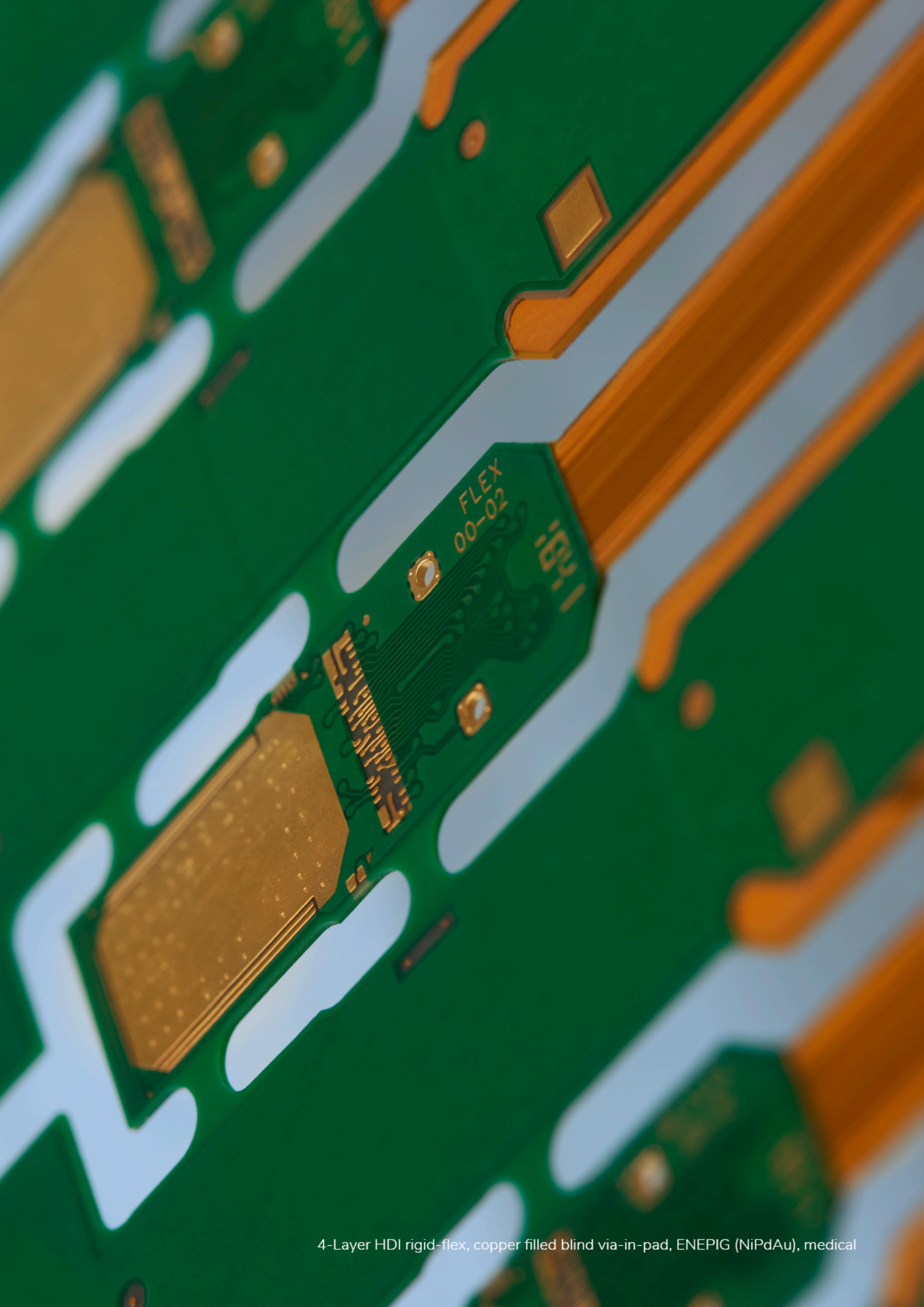
Design rules

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Ref.	Design parameter	Unit	Standard	Advanced	Development
A,B	Maximum board size	mm	630 x 620 (rigid), 570 x 417 (rigid-flex), 265 x 417 (flex)	-	-
	Maximum board thickness	mm	5		
C	Minimum board thickness (substrate thickness without Cu)	µm	25	12.5	12.5
	Maximum layer count rigid PCB	-	30, HDI: 6+N+6	ELIC	
	Maximum layer count rigid-flex PCB	-	10 - 4 flex	14 - 6 flex	20 - 8 flex
	Maximum layer count flex PCB	-	6	8	> 8
D1	Minimum through hole diameter (mechanically drilled)	µm	150 ~ 250	100	75
D2	Minimum hole diameter (laser drilled, blind & through holes)	µm	75 ~ 100	50	40
E	Minimum distance hole - hole (mechanically drilled)	µm	350	275	200
F1, D1	Minimum annular ring outer layer (mechanically drilled holes)	µm	100	75	50
F2, D2	Minimum annular ring outer layer (laser drilled holes)	µm	50	35	25
F3, D1	Minimum annular ring inner layer (mechanically drilled holes)	µm	125	100	75
F4, D2	Minimum annular ring inner layer (laser drilled holes)	µm	75	50	40
C, D1	Maximum aspect ratio through holes	D1:C	1:10	1:12	1:16
G, D2	Maximum aspect ratio blind vias (base copper included)	D2:G	1:0.8	1:0.9	1:1
H	Copper filling ratio blind holes	%	80	90	> 90
I	Minimum line width (depending on copper thickness)	µm	75	50	< 50
J	Minimum spacing (depending on copper thickness)	µm	75	50	< 50
K	Minimum soldermask opening	µm	50	40	20
L	Minimum soldermask dam width	µm	100	60	50
M	Minimum distance conductive material to board outline (mechanical/laser)	µm	150 / 100	100 / 75	75 / 50
	Layer to layer alignment	µm	+/- 50	+/-40	+/- 35
	Hole to hole alignment (laser drilled)	µm	+/- 25	+/- 20	+/-20
	Hole to hole alignment (mechanically drilled)	µm	+/- 35	+/- 30	+/- 30
	Controlled Impedance tolerance	%	+/- 10	+/- 8	+/- 5
	Automatic optical inspection (AOI)	%	100	100	100

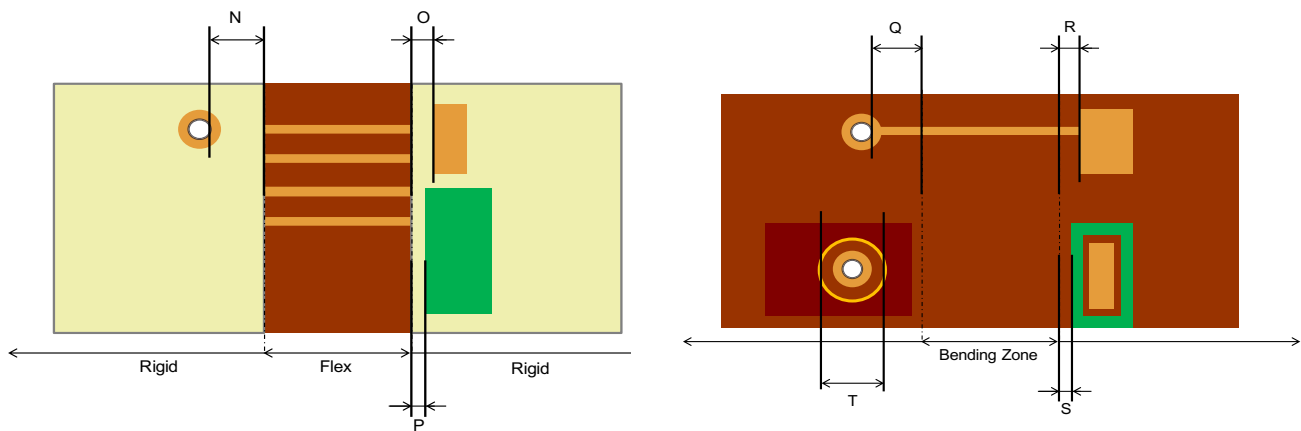
Recommended data file formats: Extended GERBER (RS-274X), ODB+, DXF, DWG.



4-Layer HDI rigid-flex, copper filled blind via-in-pad, ENEPIG (NiPdAu), medical

Design rules

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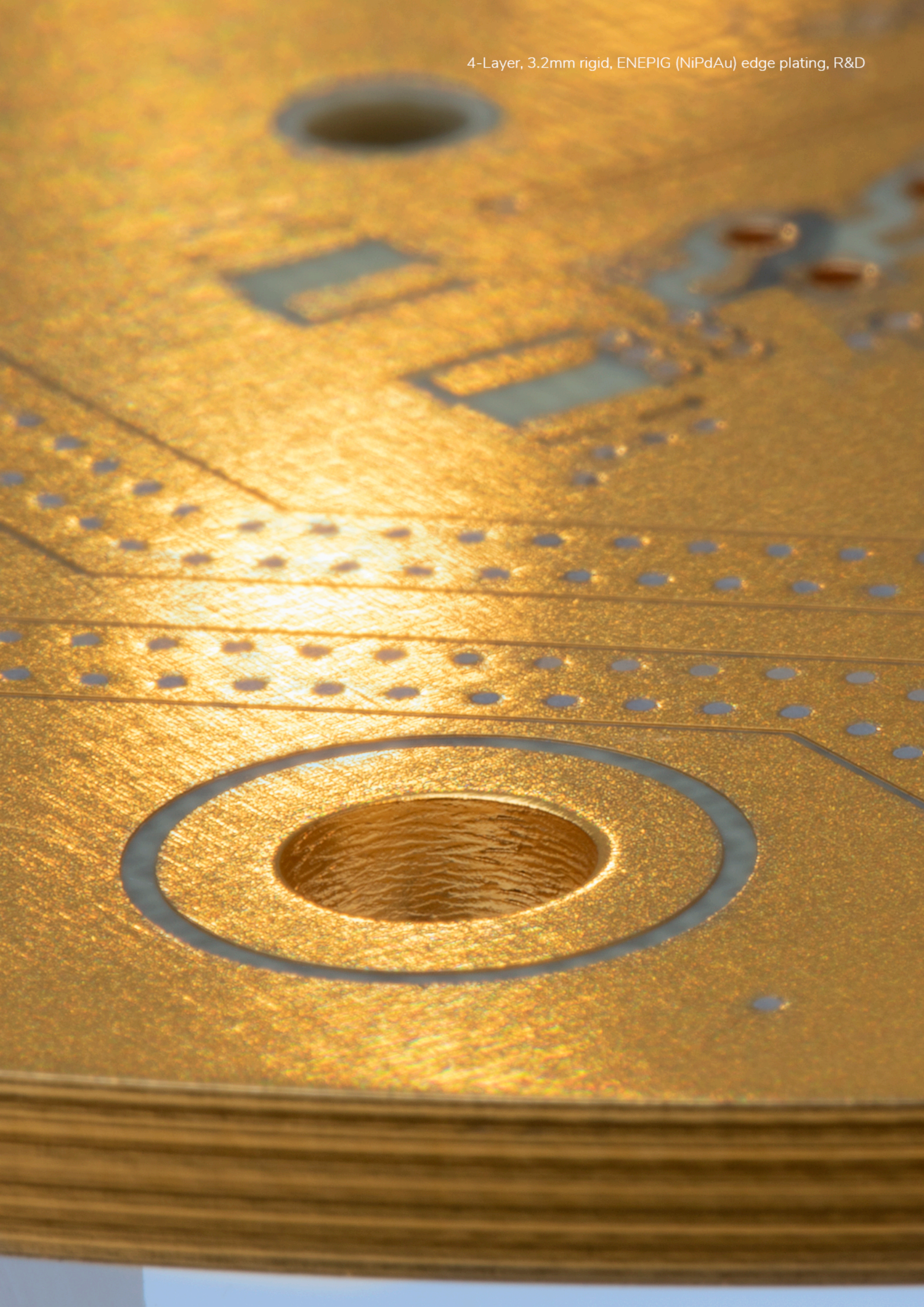
Ref.	Design parameter	Unit	Standard	Advanced	Development
N	Distance holes to transition zone rigid-flex	mm	> 1	> 0.7	> 0.5
O	Distance conductive pads to transition zone rigid-flex	mm	0.6	0.4	0.25
P	Distance soldermask to transition zone rigid-flex	µm	200	150	100
Q	Distance holes to bending zone flex	µm	400	300	200
P	Distance conductive pads to bending zone flex	µm	300	200	150
S	Distance soldermask to bending zone flex	µm	100	70	50
T	Coverlayer opening: pad size +	µm	+ 300	+ 250	+ 200

PCB – Cavity

Multi-cavity layouts are possible, depending on the boards thickness and layer count

Design parameter	Depth tolerance	Plated cavities
Depth routing	+/- 150 µm	++
Laser cavities	+/- 125 µm	++
Cavity creation by sequential lamination	+/- 10% laminate thickness	+

4-Layer, 3.2mm rigid, ENEPIG (NiPdAu) edge plating, R&D



Design rules

PCB – base materials

Material type	Designation	Tg °C	Vendor	Remarks
Standard FR4	S-1000H	150	Shengyi	Low CTE, CAF resistant, IPC-4101
	TU-662	150	TUC	Type Designation : /21, /98, /99,
	NP-155FTL	150	NanYa	/101, /121, /124
High Tg FR4	S1000-2M	180	Shengyi	Low CTE, CAF resistant, IPC-4101 Type Designation : /98, /99, /101, /121, /124, /126, /129
	IT-180A	175	ITEQ	
	TU-768	180	TUC	
	NP-175F	170	NanYa	
High frequency	4000 Series	280	Rogers	Ceramic filled substrate
	TC350	-	Rogers	
	I-Tera MT40	200	Isola	FR4 process compatible
Thermal Management	92ML	160	Rogers	Thermal conductivity= 2.0 W/m-K, 6-10x that of FR4
Polyimide Film	ThinFlex-A, -G, -H, ...	-	ThinFlex	Adhesiveless FCCL, IPC-4104 Type Designation : /11
	Pylux AP/AC	-	Dupont	
	SF202	-	Shengyi	Acrylic adhesive type FCCL
	NanPao F series	-	Nan Pao	
Coverlay	ThinFlex-I, -M, -Q, ...	-	ThinFlex	
	LF, FR	-	Dupont	
	SF305C	-	Shengyi	
	NanPao L series	-	Nan Pao	
Adhesive	ThinFlex-KC	-	ThinFlex	Acrylic adhesive type FCCL
	LF, FR	-	Dupont	
	NanPao D series	-	Nan Pao	
Stiffener	PI, FR4, Stainless steel, Aluminium			

Above listed are commonly used base materials. Basically any type of material is available upon request.
Hybrid stack-up's are possible upon request.

Design rules

PCB – surface finishes

Surface finish type	Thickness (µm)	Recommended shelf life	Soldering	Al - Wire bonding	Au - Wire bonding	Contacts/connectors
ENIG (NiAu)	Ni: 3 ~ 6 Au: 0.05 minimum	1 year	++	++	-	+
ENEPIG (NiPdAu)	Ni: 3 ~ 6 Pd: 0.05 ~ 0.15 Au: 0.05 minimum	1 year (for Au wire - bonding we recomend a shelf life of 6 months)	++	++	++	+
Electroplated Ni / soft Au	According to customer requirement	6 months	++	++	-	+
Electroplated Ni / hard Au	According to customer requirement	1 year	++	++	++	++
Immersion Tin (Sn)	1.2 max	6 months	++	-	-	-
Immersion Silver (Ag)	0.15 ~ 0.45	6 months	++	-	-	-
OSP (ENTEK HT plus)	0.2 - 0.3 - 0.5	1 year	++	-	-	-
HASL lead free	1 ~ 30	1 year	++	-	-	-

PCB – Quality assurance

Eurotronics attaches great value to quality just to ensure that only PCB's that meet your quality requirements are delivered. That's why Eurotronics has build up a long term strategic partnership with one of the finest printed circuit board production facilities in Taiwan, China and Germany to make sure high quality printed circuit board technologies are guaranteed with respect for human rights and the strictest environmental demands.

The quality management system is guaranteed by a fully integrated ERP system and well maintained calibration processes. Every single PCB is inspected according to IPC A-600H class 2 and pursuant to customer specifications. At explicit request we can even guarantee IPC Class 3.

Quality overview
Design for Manufacturing.
Verified, validated and reproducible production processes managed by a fully integrated ERP system.
ISO 9001 certified quality management systems.
ISO 14001 certified environmental quality sytems.
UL, RoHs, REACH & EICC-GeSi certified quality management systems.
Inspection & electrical testing according to IPC-A600 class 2, class 3 or specific customer specifications.
Interconnect stress test (IPC specified thermal cycle test).
End-to-end traceability of products, materials and test results.